

100

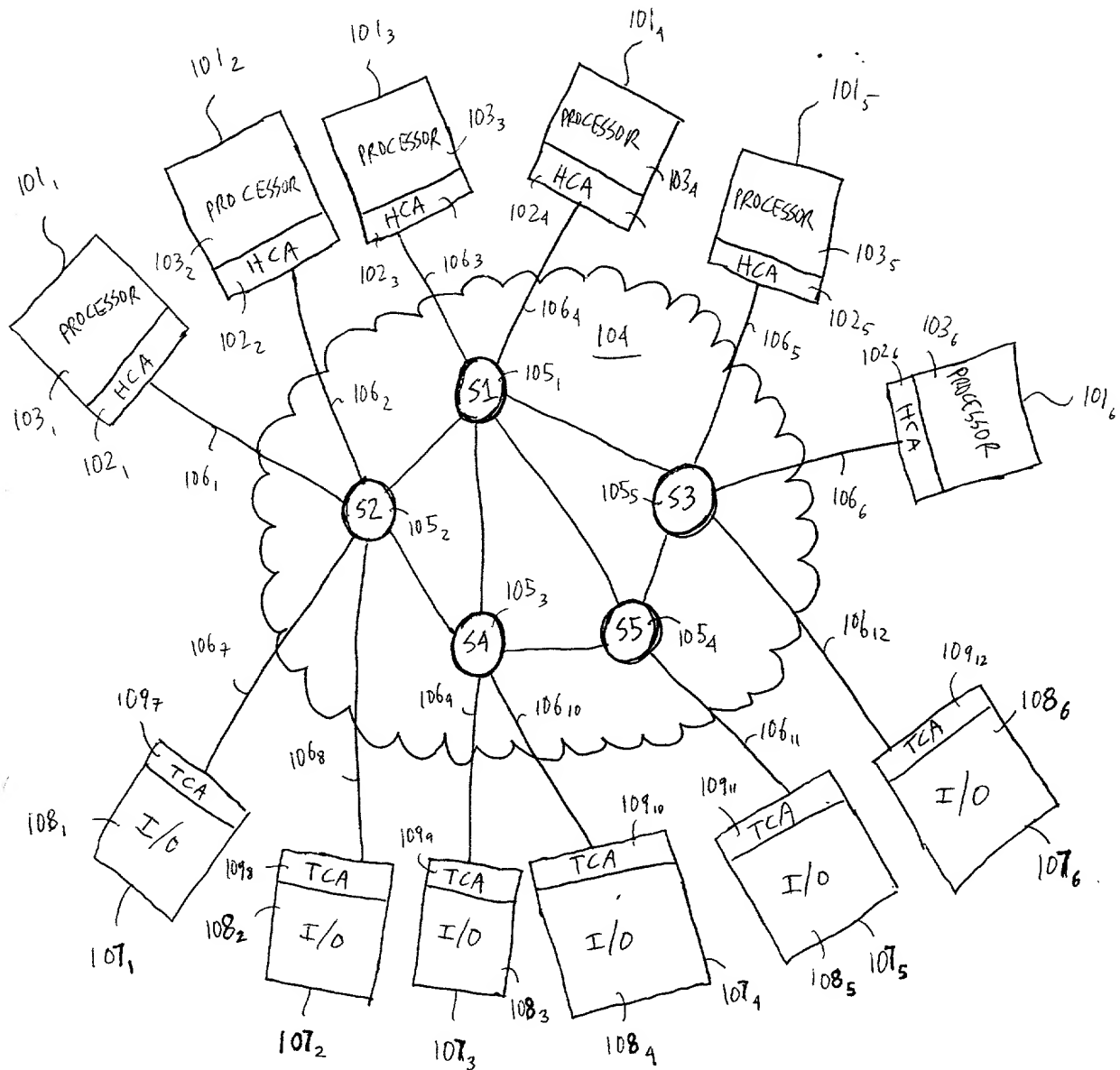
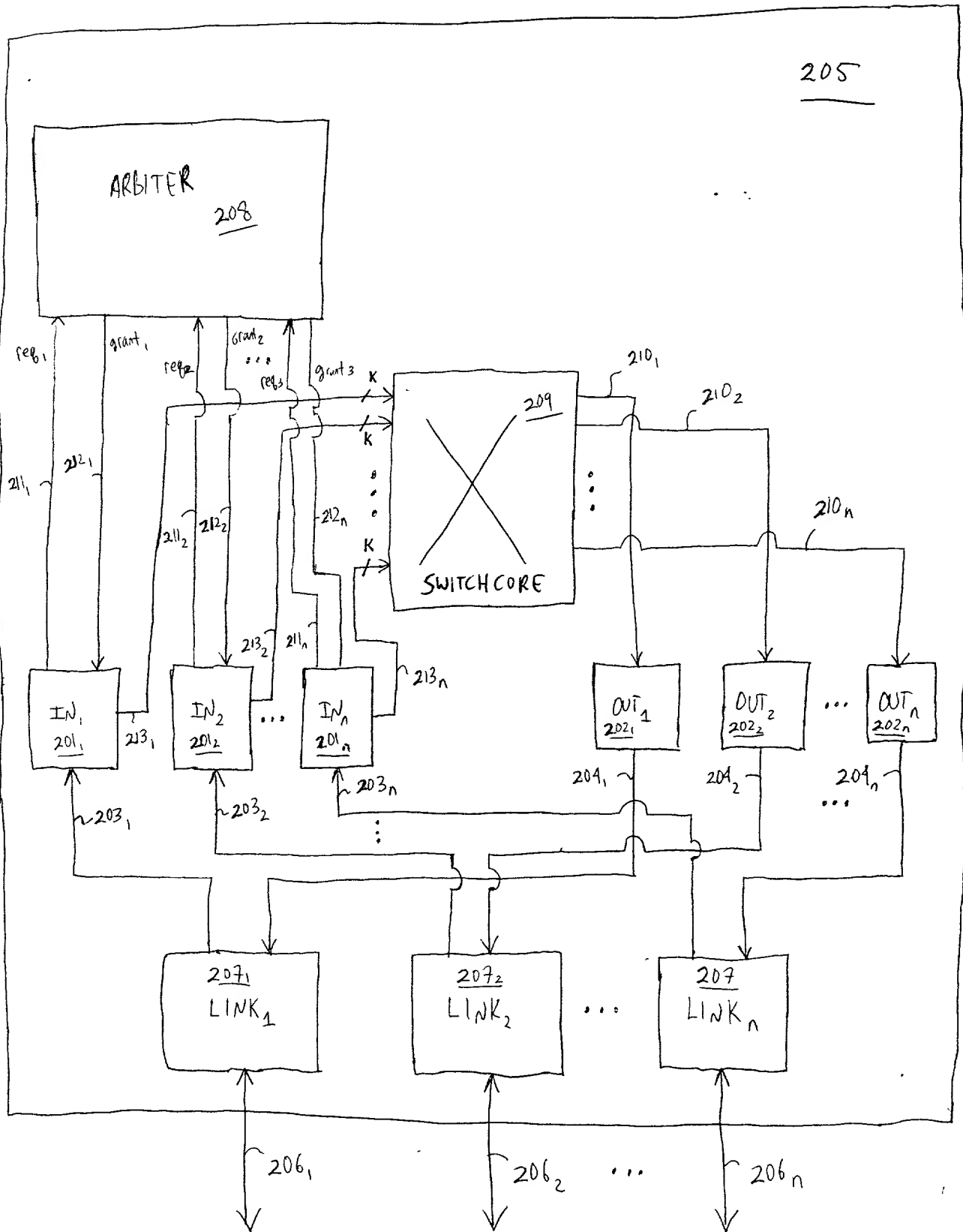


FIGURE 1

FIGURE 2



INPUT
PORT 301

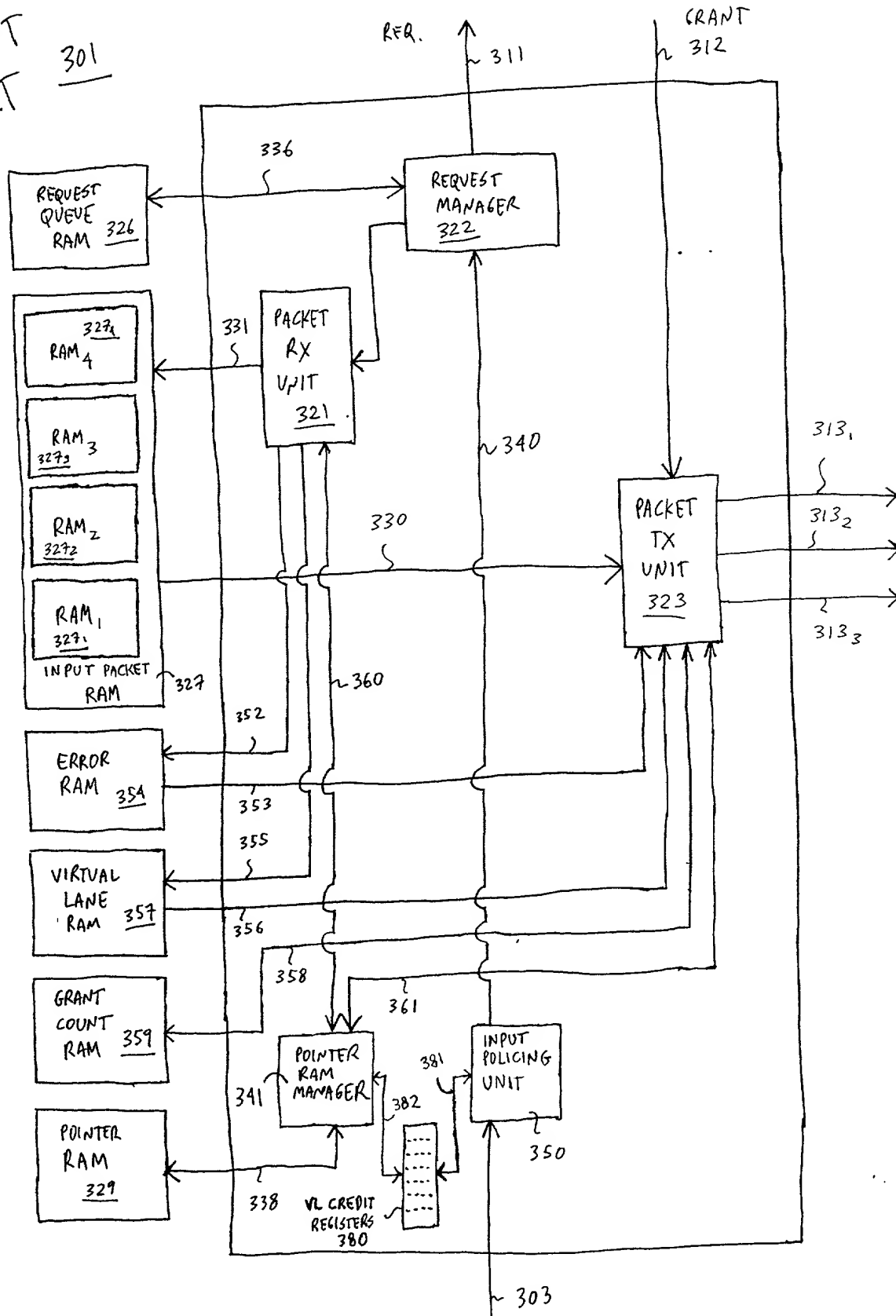


FIGURE 3

FROM LINK INTERFACE

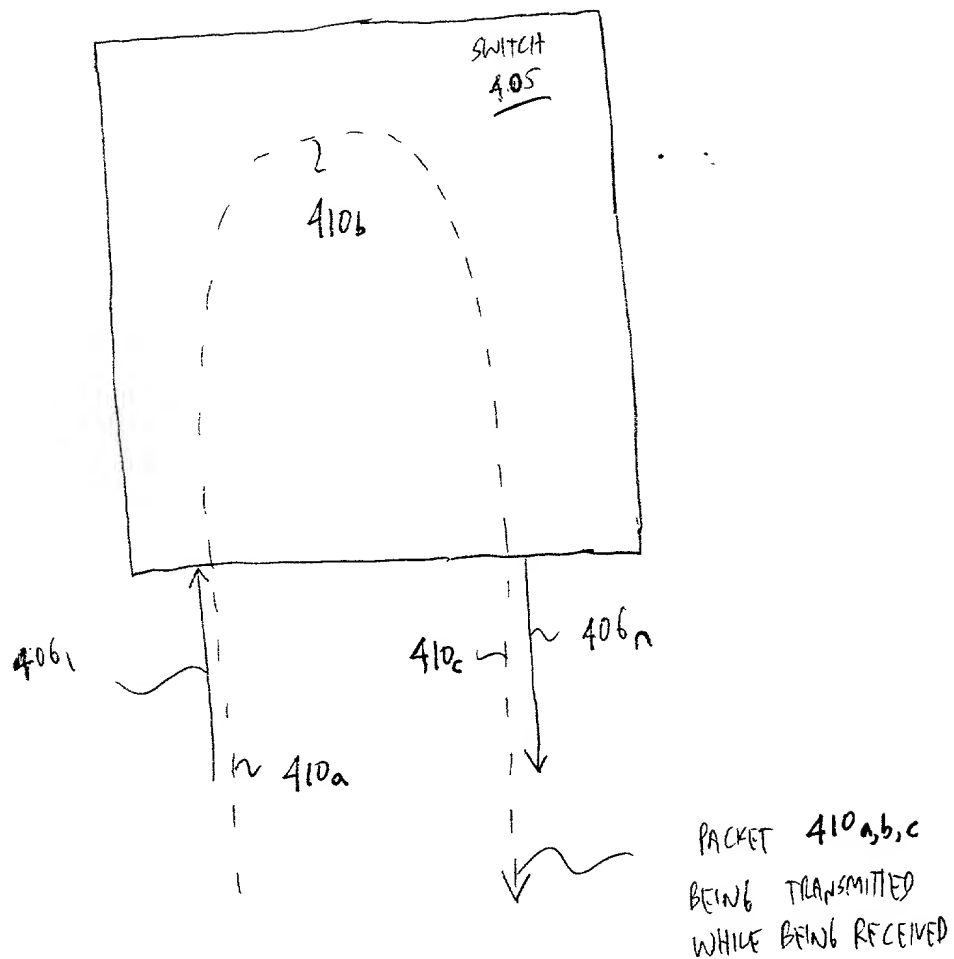


FIGURE 4

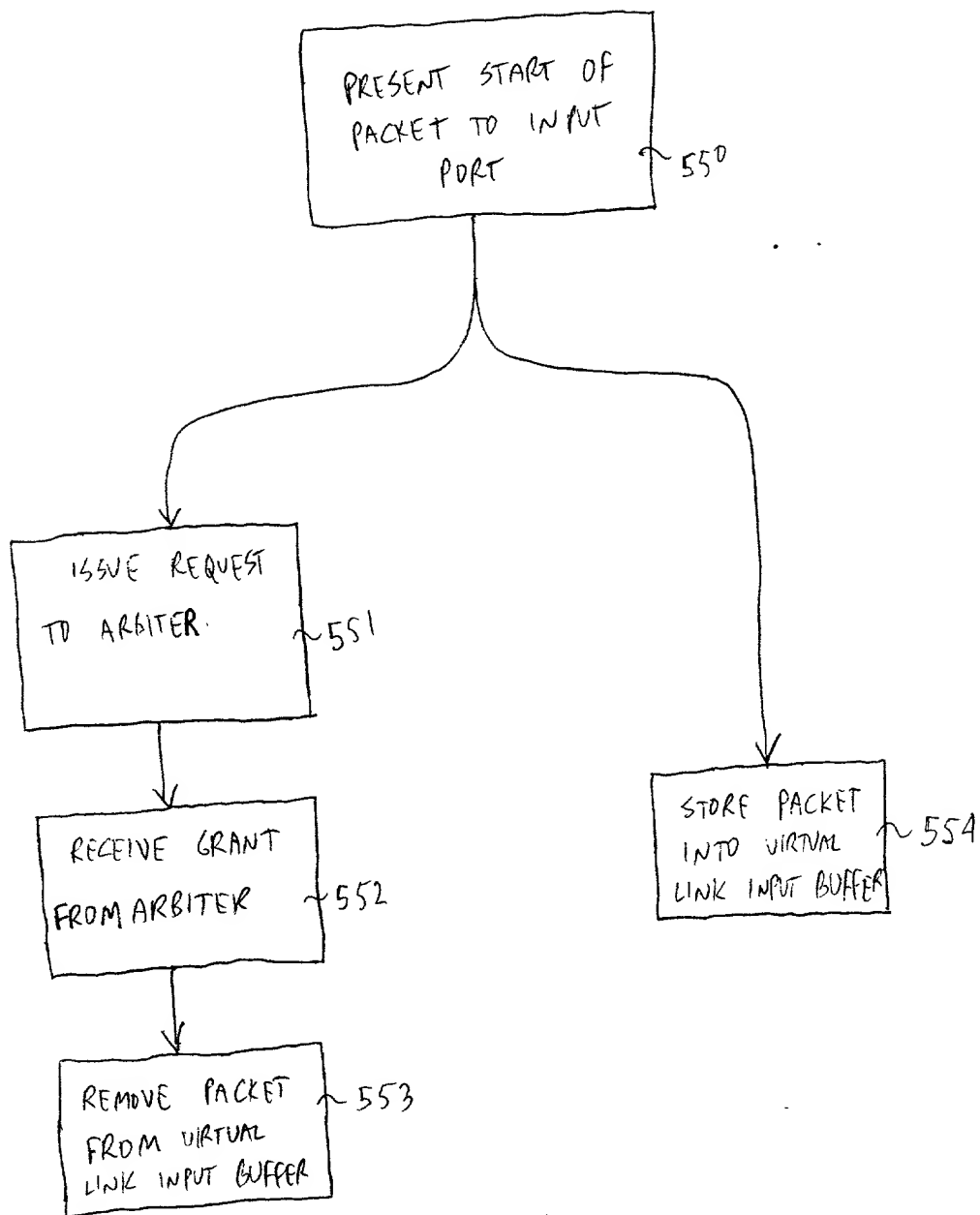


FIGURE 5

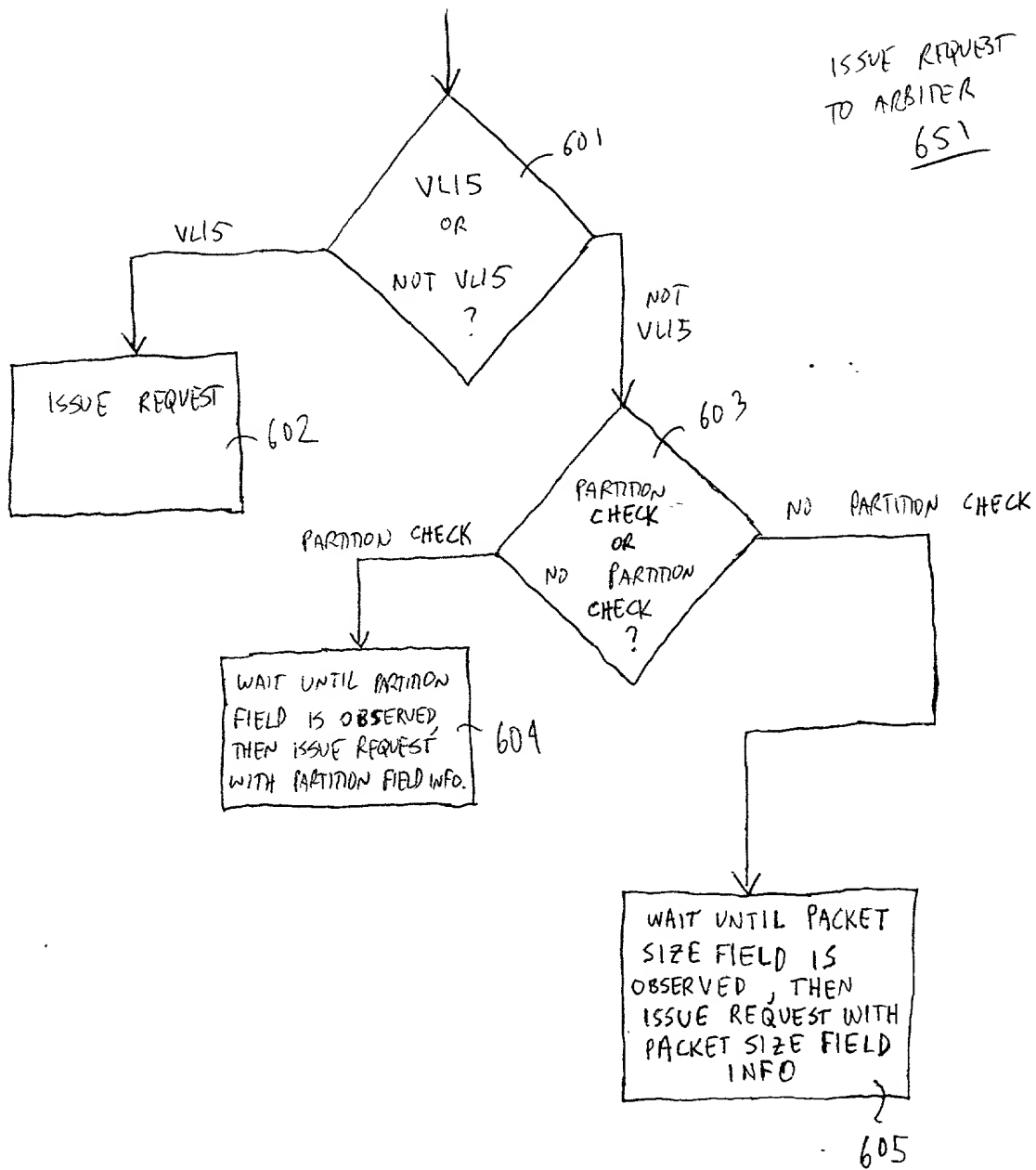


FIGURE 6

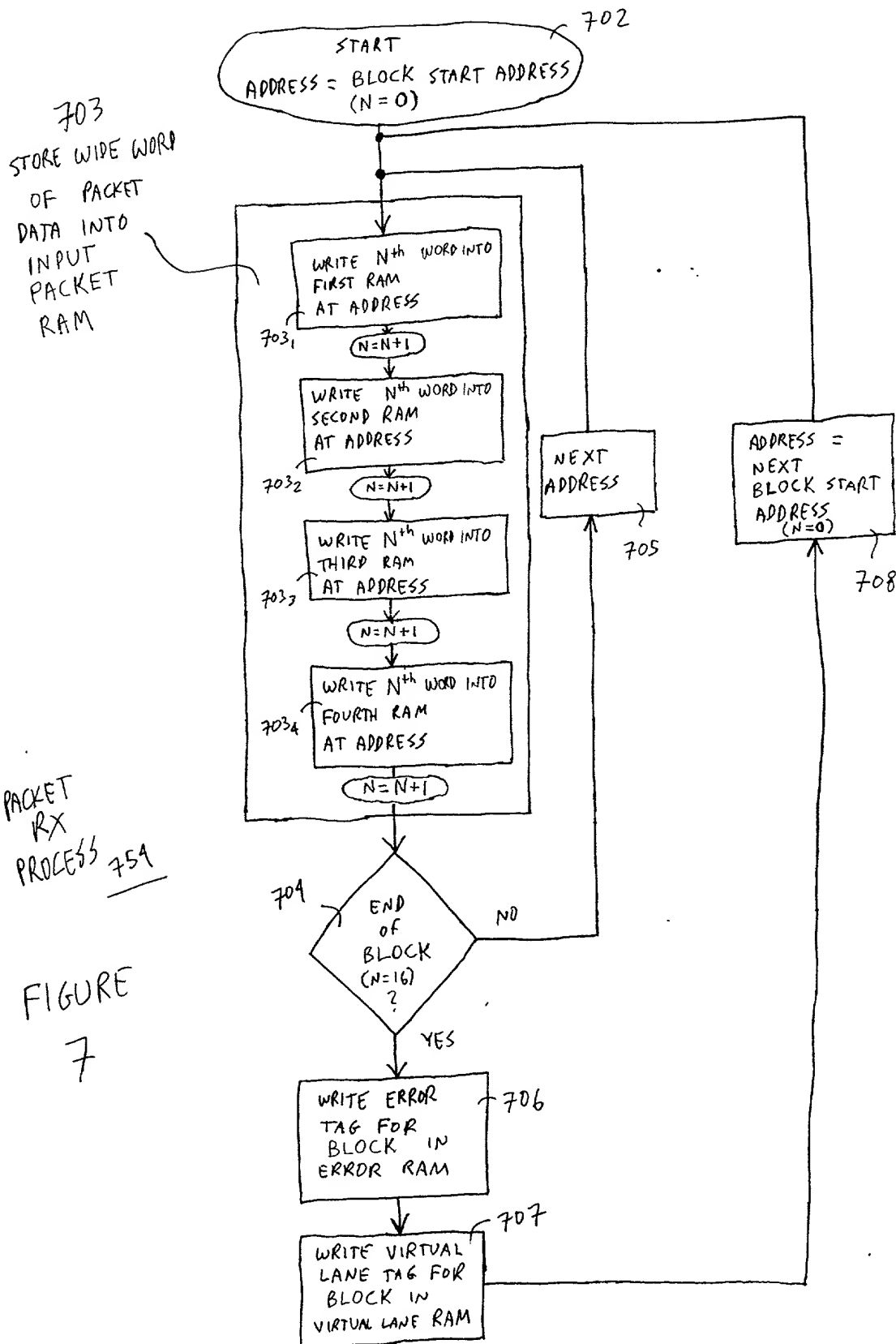


FIGURE
7

Handwritten notes on the left margin: "The diagram shows the state of the buffer at different times. The buffer is divided into two parts: ADDRESS and DATA. The ADDRESS part contains the addresses of the packets currently in the buffer. The DATA part contains the data of the packets currently in the buffer. The diagram shows the state of the buffer at times T1, T2, T3, T4, T5, T6, T7, and T8. The buffer is initially empty. At T1, the first packet arrives. At T2, the second packet arrives. At T3, the third packet arrives. At T4, the fourth packet arrives. At T5, the first packet is received. At T6, the second packet is received. At T7, the third packet is received. At T8, the fourth packet is received. The buffer is then empty.

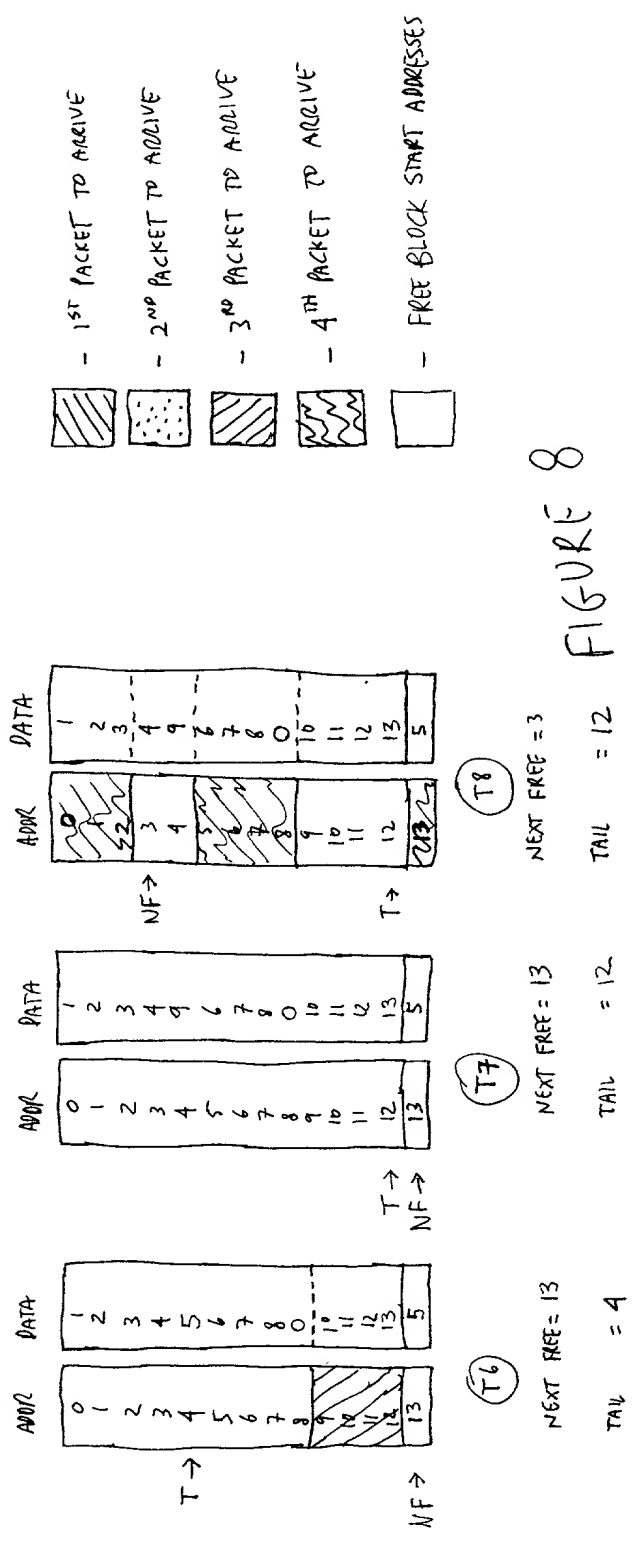
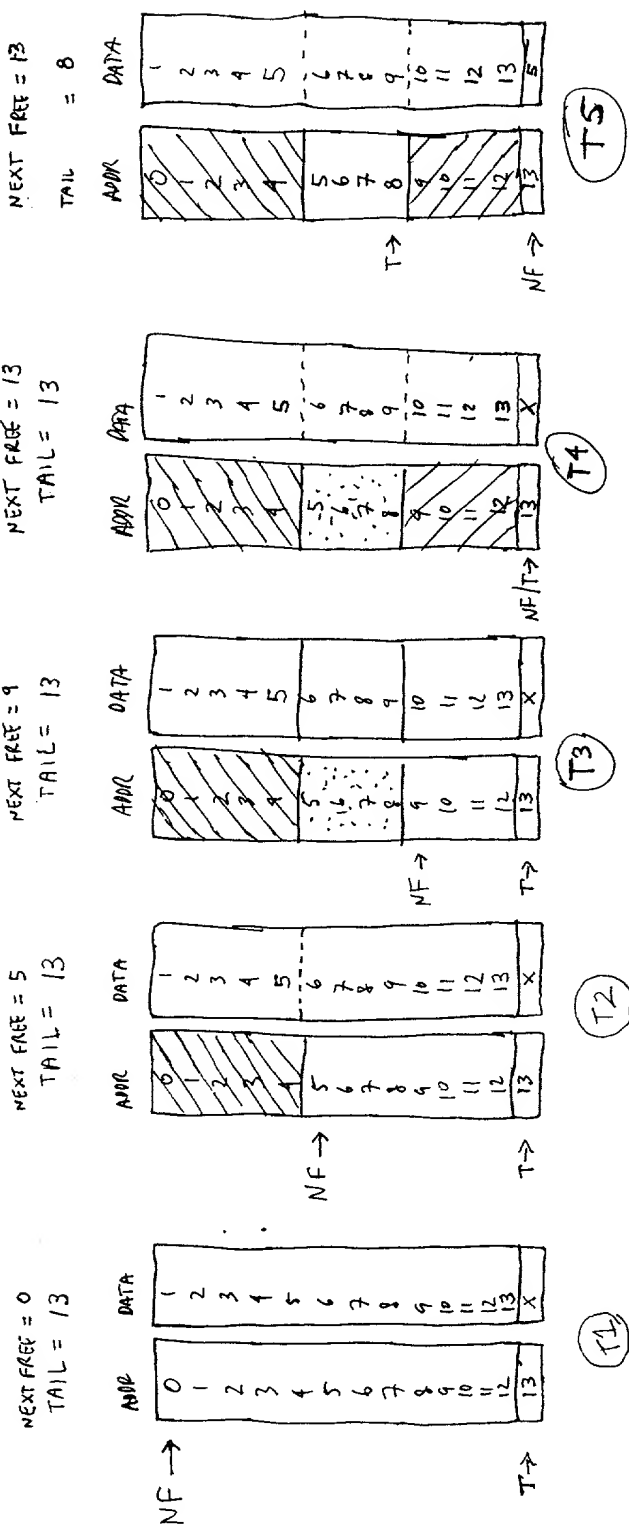


FIGURE 8

REQUEST FOR BLOCK
START ADDRESS FROM
PACKET Rx UNIT

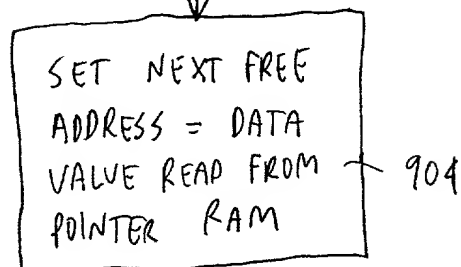
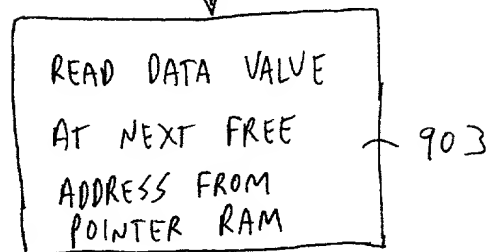
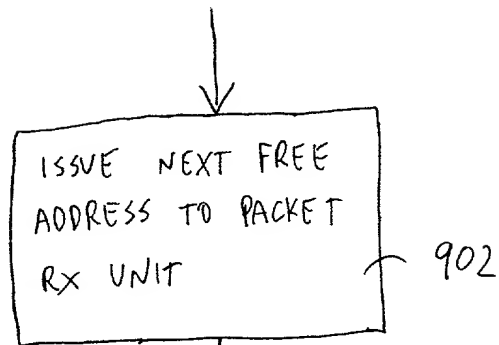


FIGURE
9A

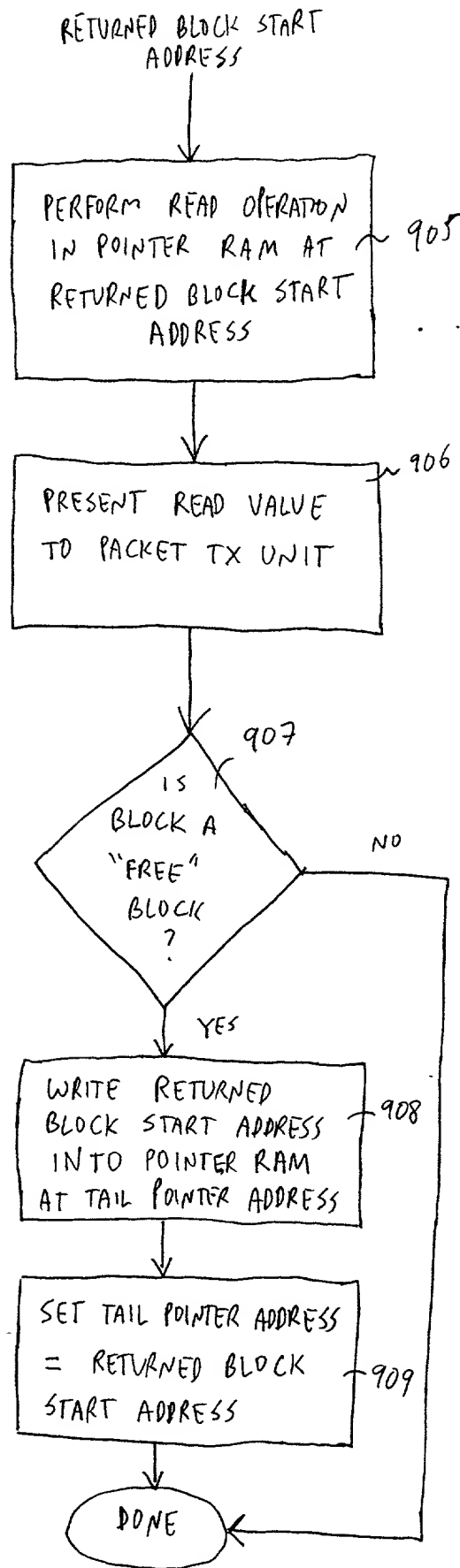
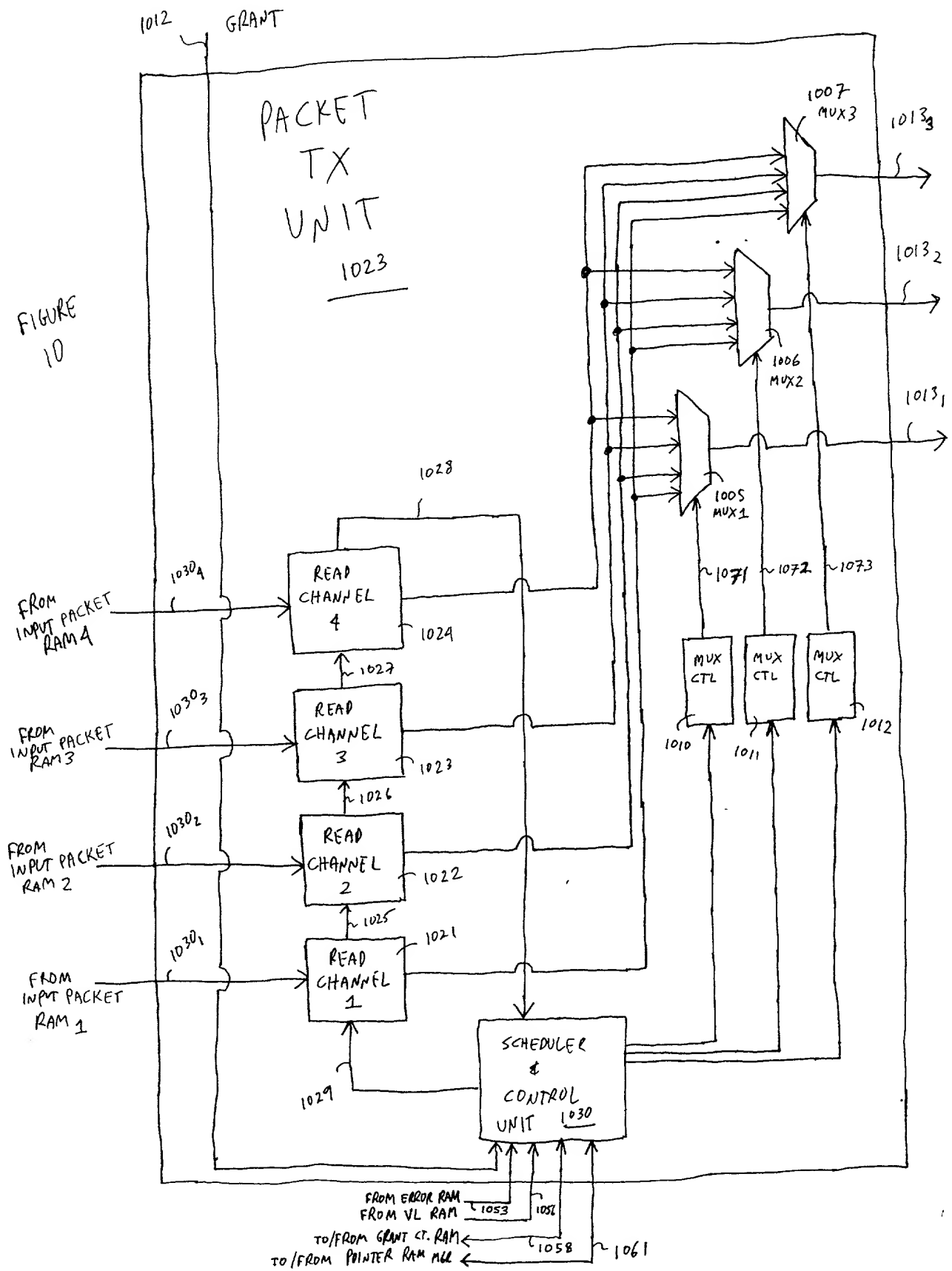


FIGURE 9B

FIGURE 10



T1	T2	T3	T4	T5	T6	T7	T8
$P1/BSA$	$P2/BSA$	$P3/BSA$		$P1/BSA(H)$	$P2/BSA(H)$	$P3/BSA(H)$	
	$P1/BSA$	$P2/BSA$	$P3/BSA$		$P1/BSA(H)$	$P2/BSA(H)$	$P3/BSA(H)$
		$P1/BSA$	$P2/BSA$	$P3/BSA$		$P1/BSA(H)$	$P2/BSA(H)$
			$P1/BSA$	$P2/BSA$	$P3/BSA$		$P1/BSA(H)$
$RC1$	$RC2$	$RC3$	$RC4$	$RC1$	$RC2$	$RC3$	$RC4$
	$RC1$	$RC2$	$RC3$	$RC4$	$RC1$	$RC2$	$RC3$
		$RC1$	$RC2$	$RC3$	$RC4$	$RC1$	$RC2$

RC1

RC2

RC3

RC4

MUX1

MUX2

MUX3

1120

1130

time \uparrow

FIGURE 11